

2244

EAST - [~~~~~1.wsp:1]

File View [?] Tools Window Help

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☒ Favorites
☒ Tagged

Search:
 DBs: USPAT, US-PG-PUB, EPO, JPO, DERWENT, IBM TDB
 Default operator: OR
☐ Plural ☐ Synonyms
☒ Highlight all hit terms initially

word-lines or word adj lines) and memory and reference adj cell\$) and redundan\$) and activ\$ same connected) and replac\$)

☒ BRS term ☒ BRS term ☒ Image ☒ Text

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
10	<input type="checkbox"/>	<input type="checkbox"/>	US 5453391 A	19950926	16	Method for manufacturing a contactless floating gate	438/263	438/261
11	<input type="checkbox"/>	<input type="checkbox"/>	US 5450361 A	19950912	81	Semiconductor memory device having redundant memory	365/200	365/189.07 ; 365/203
12	<input type="checkbox"/>	<input type="checkbox"/>	US 5399928 A	19950321	13	Negative voltage generator for flash EPROM design	327/434	326/92 ; 327/536
13	<input type="checkbox"/>	<input type="checkbox"/>	US 5399891 A	19950321	20	Floating gate or flash EPROM transistor array having	365/185.16	257/314 ; 257/315
14	<input type="checkbox"/>	<input type="checkbox"/>	US 5327383 A	19940705	43	Method and circuitry for erasing a nonvolatile	365/185.24	365/185.09 ; 365/185.12
15	<input type="checkbox"/>	<input type="checkbox"/>	US 5031151 A	19910709	14	Wordline drive inhibit circuit implementing	365/195	365/200 ; 365/210
16	<input type="checkbox"/>	<input type="checkbox"/>	US 5023839 A	19910611	6	Redundant semiconductor memory device	365/185.21	365/185.09
17	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5022006 A	19910604	14	Semiconductor memory having bit lines with isolation	365/200	365/51 ; 714/711
18	<input checked="" type="checkbox"/>	<input type="checkbox"/>	EP 1102168 A2	20011029		Integrated memory with memory cells and reference		
19	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5022006 A	19910604	14	Semiconductor memory using redundant words for repair -		

☒ Hits ☒ Details

EAST - [*****1.wsp:1]

File View [db] Tools Window Help

☐ L2: (1333759) 1 and
☐ L3: (851) 2 and ref
☐ L4: (86) 3 and redu
☐ L5: (54) 4 and redu
☐ L6: (33) 5 and acti
☐ L7: (27) 6 and sens
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[Previous] [In] [Browse] [Queue] [Clear]
 DBs: USPAT, US:PGPUB, EPD, JPO, DERWENT, IBM, TDB
 Default operator: DR
☐ Eureka ☐ Synonyms
☒ Highlight all hit terms initially
 6 and sense

☒ BRS term ☒ I&R term ☒ Image ☒ Text

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
18	<input type="checkbox"/>	<input type="checkbox"/>	US 5453391 A	19950926	16	Method for manufacturing a contactless floating gate	438/263	438/261
19	<input type="checkbox"/>	<input type="checkbox"/>	US 5399891 A	19950321	20	Floating gate or flash EPROM transistor array having	365/185.16	257/314 ; 257/315
20	<input type="checkbox"/>	<input type="checkbox"/>	US 5377147 A	19941227	42	Method and circuitry for preconditioning shorted rows	365/185.09	365/185.12 ; 365/185.21
21	<input type="checkbox"/>	<input type="checkbox"/>	US 5347489 A	19940913	41	Method and circuitry for preconditioning shorted rows	365/203	365/185.2 ; 365/185.24
22	<input type="checkbox"/>	<input type="checkbox"/>	US 5327383 A	19940705	43	Method and circuitry for erasing a nonvolatile	365/185.24	365/185.09 ; 365/185.12
23	<input type="checkbox"/>	<input type="checkbox"/>	US 5237535 A	19930817	17	Method of repairing overerased cells in a flash	365/185.3	365/185.12 ; 365/185.19
24	<input type="checkbox"/>	<input type="checkbox"/>	US 5142496 A	19920825	16	Method for measuring V.sub.T's less than zero without	365/201	365/104 ; 365/185.09
25	<input type="checkbox"/>	<input type="checkbox"/>	US <u>5031151</u> A	19910709	14	Wordline drive inhibit circuit implementing	365/195	365/200 ; 365/210
26	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US <u>5022006</u> A	19910604	14	Semiconductor memory having bit lines with isolation	365/200	365/51 ; 714/711
27	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 4874500 A	19891017	18	Microelectrochemical sensor and sensor array	204/412	204/408 ; 204/416

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Search:
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6 and sense

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6292383 B1	20010918	11	Redundant memory cell for dynamic random access	365/69	365/200 ; 365/63
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6282145 B1	20010828	74	Array architecture and operating methods for	365/230.06	365/51 ; 365/63
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6275434 B1	20010814	39	Semiconductor memory	365/206	365/208 ; 365/63
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6212096 B1	20010403	10	Data reading path management architecture for a memory	365/185.02	365/185.17
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6091655 A	20000718	39	Semiconductor memory	365/210	365/149 ; 365/189.12
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6085233 A	20000704	86	System and method for cellular network computing	709/216	709/212 ; 709/237
7	<input type="checkbox"/>	<input type="checkbox"/>	US 5961653 A	19991005	18	Processor based BIST for an embedded memory	714/7	714/30 ; 714/718
8	<input type="checkbox"/>	<input type="checkbox"/>	US 5953255 A	19990914	35	Low voltage, low current hot-hole injection erase and	365/185.29	365/185.28 ; 365/185.3
9	<input type="checkbox"/>	<input type="checkbox"/>	US 5946237 A	19990831	13	Nonvolatile memory device capable of reading data with	365/185.2	365/185.09 ; 365/185.11
10	<input type="checkbox"/>	<input type="checkbox"/>	US 5854004 A	19981229	86	Process for screening substances capable of	435/7.21	435/6 ; 435/8
11	<input type="checkbox"/>	<input type="checkbox"/>	US 5691938 A	19971125	18	Non-volatile memory cell and array architecture	365/185.11	257/316 ; 365/185.06

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
12	<input type="checkbox"/>	<input type="checkbox"/>	US 5633185 A	19970527	17	Method of making a non-volatile memory cell	438/258	438/279
13	<input type="checkbox"/>	<input type="checkbox"/>	US 5618742 A	19970408	28	Method of making flash EPROM with conductive sidewall	438/263	438/264 ; 438/267
14	<input type="checkbox"/>	<input type="checkbox"/>	US 5610867 A	19970311	14	DRAM signal margin test method	365/201	365/189.05 ; 365/189.07
15	<input type="checkbox"/>	<input type="checkbox"/>	US 5572707 A	19961105	8	Nonvolatile memory with a programmable configuration	711/170	326/38 ; 711/102
16	<input type="checkbox"/>	<input type="checkbox"/>	US 5559739 A	19960924	14	Dynamic random access memory with a simple test	365/189.01	365/201 ; 365/203
17	<input type="checkbox"/>	<input type="checkbox"/>	US 5526307 A	19960611	32	Flash EPROM integrated circuit architecture	365/185.01	257/316 ; 365/185.09
18	<input type="checkbox"/>	<input type="checkbox"/>	US 5453391 A	19950926	16	Method for manufacturing a contactless floating gate	438/263	438/261
19	<input type="checkbox"/>	<input type="checkbox"/>	US 5399891 A	19950321	20	Floating gate or flash EPROM transistor array having	365/185.16	257/314 ; 257/315
20	<input type="checkbox"/>	<input type="checkbox"/>	US 5377147 A	19941227	42	Method and circuitry for preconditioning shorted rows	365/185.09	365/185.12 ; 365/185.21
21	<input type="checkbox"/>	<input type="checkbox"/>	US 5347489 A	19940913	41	Method and circuitry for preconditioning shorted rows	365/203	365/185.2 ; 365/185.24
22	<input type="checkbox"/>	<input type="checkbox"/>	US 5327383 A	19940705	43	Method and circuitry for erasing a nonvolatile	365/185.24	365/185.09 ; 365/185.12

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